deposition and patterning as shown in FIG. 16. With improved lithography, the interpixel spacing can be reduced for a high fill factor even with small pixel sizes. The M3 106 mirror is used as a light blocking layer outside the array where M2 104 is used for wiring or outside the liquid crystal glue seal area an opaque polymer could be applied during packaging after the electrical contacts are made. The final two lithographic steps are used to form the SiO2 spacers 32 and expose the M2 104 contact and test pads. One of the key advantages of this process is that M2 104 is available outside of the array for wiring, which enables the integration of the data drivers onto the chip.

REMARKS

Reconsideration is respectfully requested in view of any changes to the claims and the remarks herein. Please contact the undersigned to conduct a telephone interview in accordance with MPEP 713.01 to resolve any remaining requirements and/or issues prior to sending another Office Action. Relevant portions of MPEP 713.01 are included on the signature page of this amendment.

In response to the objection to the drawings in Office Action dated 2-19-2002, attached are corrected drawings. Changes have been made to Fig. 7 through Fig. 10 to correct typographical errors. Element numerals have been added to Figs 12 through Fig. 17. Fig. 18 has been added to schematically show reference numerals 92, 93 and 94. Additional numerals have been added to the specification corresponding to Figs. 12 through 18. No new matter has been added. Support is found throughout the specification and drawings and in the original informal drawings submitted with the parent application, a copy of which is attached.

In view of the changes to the claims and the remarks herein, the Examiner is respectfully requested to reconsider the above-identified application. If the Examiner wishes to discuss the application further, or if additional information would be required, the undersigned will cooperate fully to assist in the prosecution of this application.

Please charge any fee necessary to enter this paper and any previous paper to deposit account 09-0468.

If the above-identified Examiner's Action is a final Action, and if the above-identified application will be abandoned without further action by applicants, applicants file a Notice of Appeal to the Board of Appeals and Interferences appealing the final rejection of the claims in the above-identified Examiner's Action. Please charge deposit account 09-0468 any fee necessary to enter such Notice of Appeal.

In the event that this amendment does not result in allowance of all such claims, the undersigned attorney respectfully requests a telephone interview at the Examiner's earliest convenience.

MPEP 713.01 states in part as follows:

> Where the response to a first complete action includes a request for an interview or a telephone consultation to be initiated by the examiner, ... the examiner, as soon as he or she has considered the effect of the response, should grant such request if it appears that the interview or consultation would result in expediting the case to a final action.

Respectfully submitted,

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APPENDIX

Replacement paragraph at the top of page 18 as follows:

The reflector/absorber layer 34 is formed by sputter deposition of 10 nm Ti, 100 nm Al(Cu), and 50 nm TiN and patterning by reactive ion etching (RIE). Layer 34 is preferably comprised of layers 92, 93 and 94 as schematically shown in Fig. 18. The bottom Ti layer 92 which is part of layer 34 shown in FIG. 7 is used for improved adhesion and contact resistance, a top or surface TiN layer 94 which is part of layer 34 shown in FIG. 7 is used as an antireflection coating, the bulk of the metallization is Al(Cu) layer 93 and metal layers 92-94 are patterned by RIE. TiN layer 94 is provided on the Al(Cu) layer 93 to reduce reflections so that fine features can be patterned by photolithography. Titanium nitride was used on the surface of reflector/absorber layer 34 since the necessary process steps were already available even though a lower red reflectivity would be desirable. One possibility would be to add carbon to the TiN: TiN0.33 C0.67 has been reported in "Optical Constants and Spectral Selectivity of Titanium Carbonitrides", by B. Karlsson, Thin Solid Films, p. 181, 87 (1982) to have a reflectivity of about 30% for all the wavelengths of interest. After the reflector/absorber layer 34 is patterned, a 400-500 nm layer of Si3 N4 is deposited to form dielectric layer 46 as shown in FIG. 7. The thickness of dielectric layer 46 is a compromise between a thinner layer for greater capacitance between reflector/absorber layer 34 and electrode/mirror 30 and a thicker layer which would reduce the probability of reflector/absorber layer 34 and electrode/mirror 30 defects and shorts.

Replacement paragraph bridging pages 21 and 22 as follows:

Starting from the Si devices 100, a total of eight masks would be needed (three metal levels M1(102), M2(104) and M3(106), three via/stud levels 50(112), 52(114) and 53(116), and two insulator levels). Starting at the S1 level 114, FIG. 12, the M2 layer 104, which is preferably formed of TiN/Al(Cu)/Ti, is patterned to function as the

reflector/absorber layer 34 within spatial light modulator array 10 and as M2 wiring outside of the array area of spatial light modulators 10 as shown in FIG. 13. The planarized SiO2 120 over electrode/mirror 30 is capped with an Si3 N4 dielectric layer 46 which is used as an etch stop between mirrors during the etching of dielectric layer 32 to form spacer posts 32 as shown in FIG. 17. Inside the spatial light modulator array 10, to get the most effective light shielding, the S2 116 stud is stacked directly on the S1 114 stud as shown in FIG. 15. Alternatively, an M2 104 segment could be interposed between the two studs but this would require a larger break in the M2/AR layer 104 which would be more likely to permit light through to the semiconductor substrate below. The M3 mirror layer 106 is formed by Al or Al(Cu) deposition and patterning as shown in FIG. 16. With improved lithography, the interpixel spacing can be reduced for a high fill factor even with small pixel sizes. The M3 106 mirror is used as a light blocking layer outside the array where M2 104 is used for wiring or outside the liquid crystal glue seal area an opaque polymer could be applied during packaging after the electrical contacts are made. The final two lithographic steps are used to form the SiO2 spacers 32 and expose the M2 104 contact and test pads. One of the key advantages of this process is that M2 104 is available outside of the array for wiring, which enables the integration of the data drivers onto the chip.